WHAT IS CLAIMED IS:

1. A level transforming circuit comprising:

a first CMOS circuit which has first and second p-channel type MOS transistor connected in series between a high voltage electricity source and first output node, and first and second n-channel type MOS transistor connected in series between said first output node and the ground, wherein gate of said first p-channel type MOS transistor functioning as a pull up switch is impressed with a first signal, wherein gate of second n-channel type MOS transistor functioning as a pull down switch is impressed with an input signal having an amplitude between a low voltage electricity source and the ground, and wherein gates of said second p-channel type MOS transistor and said first n-channel type MOS transistor are impressed with the low voltage electricity source in common;

a first intermediate circuit which has third p-channel type MOS transistor connected between the high voltage electricity source and second output node wherein its gate is impressed with said first signal, and which has third n-channel type MOS transistor connected between said second output node and the low voltage electricity source wherein its gate is impressed with said first signal;

a second intermediate circuit which has fourth p-channel type MOS transistor connected between the high voltage electricity source and the second output node wherein its gate is impressed with electric potential of second output node of said first intermediate circuit, and which has fourth n-channel type MOS transistor connected between the

third output node and the low voltage electricity source wherein its gate is impressed with electric potential of second output node, and which puts out said first signal from said third output node;

a second CMOS circuit which has fifth and sixth p-channel type MOS transistor connected in series between the high voltage electricity source and fourth output node, and which has fifth and sixth n-channel type MOS transistor connected in series between said fourth output node and the ground, wherein gate of said fifth p-channel type MOS transistor functioning as a pull up switch is impressed with a signal having electric potential of second output node of first intermediate circuit, and wherein gate of said sixth n-channel type MOS transistor functioning as a pull down switch is impressed with an inverse signal of the input signal, and wherein gates of said sixth p-channel type MOS transistor and fifth n-channel type MOS transistor are impressed with the low voltage electricity source in common, and wherein a signal having amplitude of said high voltage and ground voltage is put out from said fourth output node;

a seventh p-channel type MOS transistor which is connected between common node of first and second p-channel type MOS transistors in series and second output node N3 of said first intermediate circuit and which gate is impressed with electric potential of said first output node of first CMOS circuit;

an eighth p-channel type MOS transistor which is connected between common node of fifth and sixth p-channel type MOS transistors in series and third output node of said second intermediate circuit and which gate is impressed with electric potential of said fourth output node of second CMOS circuit.

2. A level transforming circuit according to Claim 1: wherein

turning on resistance of said first p-channel type MOS transistor in said first CMOS circuit is set higher than turning on resistance of said second p-channel type MOS transistor, and turning on resistance of said second n-channel type MOS transistor is set higher than turning on resistance of said first n-channel type MOS transistor;

turning on resistance of said fifth p-channel type MOS transistor in said second CMOS circuit is set higher than turning on resistance of said sixth p-channel type MOS transistor, and turning on resistance of said sixth n-channel type MOS transistor is set higher than turning on resistance of said fifth n-channel type MOS transistor;

turning on resistance of said third p-channel type MOS transistor in said first intermediate circuit is set higher than turning on resistance of said seventh p-channel type MOS transistor; and

turning on resistance of said fourth p-channel type MOS transistor in said second intermediate circuit is set higher than turning on resistance of said eighth p-channel type MOS transistor.

3. A level transforming circuit according to Claim 1: wherein

substrate of said third n-channel type MOS transistor in said first intermediate circuit is connected with source of said third n-channel type MOS transistor, and substrate of said fourth n-channel type MOS transistor in said second intermediate circuit is connected with source of said fourth n-channel type MOS transistor; isolated from substrate of said first, second, fifth and sixth n-channel type MOS transistor.

4. A level transforming circuit according to Claim 1: wherein

substrates of said seventh p-channel type MOS transistor and an eighth p-channel type MOS transistor are connected with each source or each drain; isolated from substrate of said first to sixth n-channel type MOS transistor.

5. A level transforming circuit according to Claim 1: wherein

said first to eighth p-channel type MOS transistors and said first to sixth n-channel type MOS transistor are formed on an active region isolated by insulating film.

6. A level transforming circuit according to Claim 1: wherein

said first signal is a signal having amplitude between the high voltage and the low voltage, and said first signal is put out independently of said output signal.

7. A level transforming circuit comprising:

a first CMOS circuit which has first and second p-channel type MOS transistor connected in series between a high voltage electricity source and first output node, and first and second n-channel type MOS transistor connected in series between said first output node and the ground, wherein gate of said first p-channel type MOS transistor functioning as a pull up switch is impressed with a first signal, wherein gate of second n-channel type MOS transistor functioning as a pull down switch is impressed with an input signal having an amplitude between a low voltage electricity source and the ground, and wherein

gates of said second p-channel type MOS transistor and said first n-channel type MOS transistor are impressed with the low voltage electricity source in common;

a first intermediate circuit which has third p-channel type MOS transistor connected between the high voltage electricity source and second output node wherein its gate is impressed with said first signal, and which has third n-channel type MOS transistor connected between said second output node and the low voltage electricity source wherein its gate is impressed with said first signal;

a second intermediate circuit which has fourth p-channel type MOS transistor connected between the high voltage electricity source and the second output node wherein its gate is impressed with electric potential of second output node of said first intermediate circuit, and which has fourth n-channel type MOS transistor connected between the third output node and the low voltage electricity source wherein its gate is impressed with electric potential of second output node, and which puts out said first signal from said third output node;

a second CMOS circuit which has fifth and sixth p-channel type MOS transistor connected in series between the high voltage electricity source and fourth output node, and which has fifth and sixth n-channel type MOS transistor connected in series between said fourth output node and the ground, wherein gate of said fifth p-channel type MOS transistor functioning as a pull up switch is impressed with a signal having electric potential of second output node of first intermediate circuit, and wherein gate of said sixth n-channel type MOS transistor functioning as a pull down switch is impressed with an inverse signal of the input signal, and wherein gates of said sixth p-channel type MOS

transistor and fifth n-channel type MOS transistor are impressed with the low voltage electricity source in common, and wherein a signal having amplitude of said high voltage and ground voltage is put out from said fourth output node;

a seventh p-channel type MOS transistor which is connected between common node of first and second p-channel type MOS transistors in series and second output node of said first intermediate circuit and which gate is impressed with electric potential of said low voltage;

an eighth p-channel type MOS transistor which is connected between common node of fifth and sixth p-channel type MOS transistors in series and third output node of said second intermediate circuit and which gate is impressed with electric potential of said low voltage.

8. A level transforming circuit according to Claim 7: wherein

turning on resistance of said first p-channel type MOS transistor in said first CMOS circuit is set higher than turning on resistance of said second p-channel type MOS transistor, and turning on resistance of said second n-channel type MOS transistor is set higher than turning on resistance of said first n-channel type MOS transistor;

turning on resistance of said fifth p-channel type MOS transistor in said second CMOS circuit is set higher than turning on resistance of said sixth p-channel type MOS transistor, and turning on resistance of said sixth n-channel type MOS transistor is set higher than turning on resistance of said fifth n-channel type MOS transistor;

turning on resistance of said third p-channel type MOS

transistor in said first intermediate circuit is set higher than turning on resistance of said seventh p-channel type MOS transistor; and

turning on resistance of said fourth p-channel type MOS transistor in said second intermediate circuit is set higher than turning on resistance of said eighth p-channel type MOS transistor.

9. A level transforming circuit according to Claim 7: wherein

substrate of said third n-channel type MOS transistor in said first intermediate circuit is connected with source of said third n-channel type MOS transistor, and substrate of said fourth n-channel type MOS transistor in said second intermediate circuit is connected with source of said fourth n-channel type MOS transistor; isolated from substrate of said first, second, fifth and sixth n-channel type MOS transistor.

10. A level transforming circuit according to Claim 7: wherein

substrates of said seventh p-channel type MOS transistor and an eighth p-channel type MOS transistor are connected with each source or each drain; isolated from substrate of said first to sixth n-channel type MOS transistor.

11. A level transforming circuit according to Claim 7: wherein

said first to eighth p-channel type MOS transistors and said first to sixth n-channel type MOS transistor are formed on an active region isolated by insulating film.

12. A level transforming circuit according to Claim 7: wherein

said first signal is a signal having amplitude between the high voltage and the low voltage, and said first signal is put out independently of said output signal.

13. A level transforming circuit comprising:

a first CMOS circuit which has first and second p-channel type MOS transistor connected in series between a high voltage electricity source and first output node, and first and second n-channel type MOS transistor connected in series between said first output node and the ground, wherein gate of said first p-channel type MOS transistor functioning as a pull up switch is impressed with a first signal, wherein gate of second n-channel type MOS transistor functioning as a pull down switch is impressed with an input signal having an amplitude between a low voltage electricity source and the ground, and wherein gates of said second p-channel type MOS transistor and said first n-channel type MOS transistor are impressed with the low voltage electricity source in common;

a first intermediate circuit which has third p-channel type MOS transistor connected between the high voltage electricity source and second output node wherein its gate is impressed with said first signal, and which has third n-channel type MOS transistor connected between said second output node and the low voltage electricity source wherein its gate is impressed with said first signal;

a second intermediate circuit which has fourth p-channel type MOS transistor connected between the high voltage electricity source and the second output node wherein its gate is impressed with electric potential of second output node of said first intermediate circuit, and

which has fourth n-channel type MOS transistor connected between the third output node and the low voltage electricity source wherein its gate is impressed with electric potential of second output node, and which puts out said first signal from said third output node;

a second CMOS circuit which has fifth and sixth p-channel type MOS transistor connected in series between the high voltage electricity source and fourth output node, and which has fifth and sixth n-channel type MOS transistor connected in series between said fourth output node and the ground, wherein gate of said fifth p-channel type MOS transistor functioning as a pull up switch is impressed with a signal having electric potential of second output node of first intermediate circuit, and wherein gate of said sixth n-channel type MOS transistor functioning as a pull down switch is impressed with an inverse signal of the input signal, and wherein gates of said sixth p-channel type MOS transistor and fifth n-channel type MOS transistor are impressed with the low voltage electricity source in common, and wherein a signal having amplitude of said high voltage and ground voltage is put out from said fourth output node;

a seventh n-channel type MOS transistor which is connected between common node of first and second p-channel type MOS transistors in series and second output node of said first intermediate circuit and which gate is impressed with electric potential of said high voltage;

an eighth n-channel type MOS transistor which is connected between common node of fifth and sixth p-channel type MOS transistors in series and third output node of said second intermediate circuit and which gate is impressed with electric potential of said high

voltage.

14. A level transforming circuit according to Claim 13: wherein

turning on resistance of said first p-channel type MOS transistor in said first CMOS circuit is set higher than turning on resistance of said second p-channel type MOS transistor, and turning on resistance of said second n-channel type MOS transistor is set higher than turning on resistance of said first n-channel type MOS transistor;

turning on resistance of said fifth p-channel type MOS transistor in said second CMOS circuit is set higher than turning on resistance of said sixth p-channel type MOS transistor, and turning on resistance of said sixth n-channel type MOS transistor is set higher than turning on resistance of said fifth n-channel type MOS transistor;

turning on resistance of said third p-channel type MOS transistor in said first intermediate circuit is set higher than turning on resistance of said seventh n-channel type MOS transistor; and

turning on resistance of said fourth p-channel type MOS transistor in said second intermediate circuit is set higher than turning on resistance of said eighth n-channel type MOS transistor.

15. A level transforming circuit according to Claim 13: wherein

substrate of said third n-channel type MOS transistor in said first intermediate circuit is connected with source of said third n-channel type MOS transistor, and substrate of said fourth n-channel type MOS transistor in said second intermediate circuit is connected with source of said fourth n-channel type MOS transistor; isolated from substrate of said first, second, fifth and sixth n-channel type MOS

transistor.

16. A level transforming circuit according to Claim 13: wherein

substrates of said seventh n-channel type MOS transistor and an eighth n-channel type MOS transistor are connected with each source or each drain; isolated from substrate of said first to sixth n-channel type MOS transistor.

17. A level transforming circuit according to Claim 13: wherein

said first to sixth p-channel type MOS transistors and said first to eighth n-channel type MOS transistor are formed on an active region isolated by insulating film.

18. A level transforming circuit according to Claim 13: wherein

said first signal is a signal having amplitude between the high voltage and the low voltage, and said first signal is put out independently of said output signal.